IN THE CLAIMS

Please cancel Claims 18-22 and 25 without prejudice, and amend Claims 1, 7, 9, 31, 37-44 and 46 as follows:

1. (Currently amended) A processor interface device used in an extensible processor, comprising:

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

a data transfer fabric adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

wherein said extensible processor comprises a processor core, the configuration of which is determined based at least in part on said processor interface device.

2. (Original) The processor interface device of Claim 1, wherein said data transfer fabric comprises a crossbar switch fabric.

3. (Original) The processor interface device of Claim 1, further comprising a macro function in data communication with said at least one function port, said macro function being controlled at least in part by a processor instruction associated with said macro function, wherein said macro function may access said at least one memory port.

4. (Original) The processor interface device of Claim 1, further comprising a plurality of macro functions in data communication with respective ones of said function ports, said interface device further adapted to allow simultaneous access of multiple ones of said memory ports by respective ones of said macro functions via said function ports.

5. (Original) The processor interface device of Claim 4, wherein said at least one of said macro functions is controlled by at least one processor instruction associated with an instruction set of a host processor.

6. (Original) The processor interface device of Claim 5, wherein said host processor comprises an extensible RISC processor, and said instruction set comprises an extended instruction set thereof.

7. (Currently amended) The processor interface device of Claim 6 ~~5~~, wherein said data transferred from said storage device via said interface device is processed in pipeline fashion by at least two of said plurality of macro functions.

8. (Previously presented) The interface device of Claim 7, wherein said act of processing in pipeline fashion comprises:

assigning each of said at least two macro functions as particular stages in a pipeline; and

sequentially processing said data in said stages of said pipeline.

9. (Currently amended) A user-configured processing device, comprising:

a first data processor having an instruction set associated therewith;

a second data processor adapted to process data in a predetermined manner;

a memory array having at least one memory bank, said at least one memory bank being adapted to store a plurality of data; and

a memory interface, said memory interface having at least one first port adapted for data communication between said interface and said memory array, and at least one second port adapted for data communication between said interface and said second processor;

wherein access to said memory array via said at least one memory port is controlled at least in part by said second data processor; and

wherein at least a portion of said processing device comprises extension hardware selected by said user at time of design of said processing device, the configuration of said first data processor being based at least in part on said selected extension hardware .

10. (Original) The device of Claim 9, further comprising an arbitration unit which arbitrates access to said at least one memory bank during said access to said memory array.

11. (Original) The device of Claim 9, wherein said at least one function port further comprises at least one function controller having a plurality of registers.

12. (Original) The device of Claim 11, wherein said plurality of registers comprises registers selected from the group comprising control, status, and test registers.

13. (Original) The device of Claim 11, wherein said at least one function controller further comprises an interface to at least one pipeline stage of said first data processor.

14. (Original) The device of Claim 9, further comprising a crossbar adapted for data communication between said at least one memory port and said at least one function port.

15. (Original) The device of Claim 14, wherein said crossbar permits simultaneous access to each of said at least one memory ports by at least one of said at least one function ports.

16. (Original) The device of Claim 9, wherein said second data processor comprises a digital signal processor, said digital signal processor being optimized for calculation based on at least one predetermined algorithm.

17. (Original) The device of Claim 9, wherein said second data processor comprises an application specific integrated circuit (ASIC).

18.-30. (Cancelled)

31. (Currently amended) A ~~user-configurable~~ processor having a processor interface device associated therewith, said processor having a configuration determined at least in part by a user, comprising:

a processor core in operative communication with said interface device;

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

a data transfer fabric adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

wherein at least a portion of said interface comprises extension hardware selectively added by said user at time of said configuration; and

wherein a configuration of said processor core is based at least in part on said extension hardware.

32. (Previously presented) The processor of Claim 31, further comprising a macro function in data communication with said at least one function port, said macro function being controlled at least in part by a processor extension instruction associated with said macro function, wherein said macro function may access said at least one memory port, said extension instruction being selected by said user at said time of configuration.

33. (Previously presented) The processor interface device of Claim 31, further comprising a plurality of macro functions in data communication with respective ones of said function ports, said interface device further adapted to allow simultaneous access of multiple ones of said memory ports by respective ones of said macro functions via said function ports.

34. (Previously presented) The processor interface device of Claim 33, wherein said at least one of said macro functions is controlled by at least one processor instruction associated with an instruction set of a host processor.

35. (Previously presented) The processor interface device of Claim 34, wherein said data transferred from said storage device via said interface device is processed in pipeline fashion by at least two of said plurality of macro functions.

36. (Previously presented) The interface device of Claim 35, wherein said act of processing in pipeline fashion comprises:

assigning each of said at least two macro functions as particular stages in a pipeline; and

sequentially processing said data in said stages of said pipeline.

37. (Currently amended) A user-configurable processor device having a standardized processor interface device and configurable digital signal processor (DSP) ~~DSP~~ core associated therewith, comprising:

a processor core in operative communication with said interface device;

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

a data transfer fabric adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

wherein at least a portion of said interface comprises extension hardware selectively added by said user at time of said configuration;

wherein one or more aspects of the configuration of said processor core is based at least in part on the selection of said extension hardware; and

wherein said standardized interface is adapted to interface with any of a plurality of different configurations of said DSP core selected by said user at said time.

38. (Currently amended) The processor device of Claim 37, further comprising an software wrapper associated with said DSP core to translate at least some signals exchanged between said DSP core and said standardized interface.

39. (Currently amended) The processor device of Claim 38, wherein said software wrapper comprises an HDL (hardware description language) wrapper, said HDL wrapper being configured at least in part at said time.

40. (Currently amended) A user-configurable processor having a standardized processor interface device and ~~user-configurable~~ digital signal processing (DSP) ~~DSP~~ core associated therewith, said DSP core having a configuration determined at least in part by a user selection of extension functions, comprising:

a reduced instruction set computer (RISC) ~~RISC~~ core in operative communication with said interface device;

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

a data transfer fabric adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

wherein said standardized interface is adapted to interface with any of a plurality of different configurations of said DSP core selected by said user at the time of determining said configuration ~~said user-configuration~~.

41. (Currently amended) A user-configurable processing device having a user-configured processor interface device and digital signal processing (DSP) ~~DSP~~ core associated therewith, comprising:

a reduced instruction set computer (RISC) ~~RISC~~ core in operative communication with said interface device;

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

a data transfer fabric adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

wherein said DSP core is specifically configured by said user to inter-operate with ~~said interface~~ at least one of (i) the instruction and operand decode mechanism, (ii) auxiliary register, and (iii) on-core memory resources of said RISC processor.

42. (Currently amended) A processor device having a processor interface device associated therewith, comprising:

a processor core in operative communication with said interface device;

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

at least one function controller operatively coupled to said at least one function port, said controller being adapted to control at least one aspect of the operation of said at least one port;

a data transfer fabric adapted to transfer data and signals between said at least one memory port and said at least one function port,

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

wherein said processor core comprises a configuration determined at least in part based on user selections, said selections causing a prototype core description to be modified in order to produce said configuration.

43. (Currently amended) A user-configurable processing device having a first processor core, a user-configured processor interface device, and second core associated therewith, the interface comprising:

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port and associated function controller, said at least one function port and controller cooperating to transfer data and signals to and from a macro function;

a data transfer medium adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

wherein said second processor core is specifically configured by said user at time of design to inter-operate with ~~said interface~~ the instruction and operand decode mechanism, auxiliary register, and on-core memory resources of said first processor core.

44. (Currently amended) An processing device, comprising:

at least one extended processor core, said processor core having both base and extension instruction sets;

at least one memory port, said at least one memory port adapted to transfer data and signals to and from a storage device;

at least one function port, said at least one function port adapted to transfer data and signals to and from a macro function;

a macro function in data communication with said at least one function port, said macro function being controlled at least in part by a user-selected instruction within said extension instruction set, wherein said macro function may access said at least one memory port;

a data transfer apparatus adapted to transfer data and signals between said at least one memory port and said at least one function port, and

an arbitration unit adapted to arbitrate access to various portions of said storage device by said macro function;

wherein the design of said processor core is determined at least in part based on user selections regarding configuration of said core and at least one instruction of said extension instruction set.

45. (Previously presented) The processing device of Claim 44, wherein said processor core, memory port, function port, macro function, data transfer apparatus and arbitration unit are all disposed on a single die.

46. (Currently amended) Data processing apparatus, comprising:

an extended reduced instruction set computer (RISC) ~~RISC processor~~ core having base and extension instruction sets;

a memory interface;

a signal processing macro function optimized to perform a particular processing algorithm;

an XY memory array; and

an I/O interface;

wherein said RISC ~~processor~~ core and said macro function are coupled such that said macro function and said memory interface substantially comprise at least a portion of RISC ~~processor's~~ core's instruction set, said macro function being controlled at least in part by decoded instructions generated by the pipeline decode stage of the RISC ~~processor~~ core; and

wherein one or more peripheral devices operatively coupled to said I/O interface are provided direct memory access (DMA) capability to said XY memory array; and

wherein user selections relating to said extension instruction set made at the time of design of said RISC core are used to generate a hardware description language (HDL)

representation of at least said RISC core, said HDL representation being different than would result if different ones of said user selections were made.